REMARKS

A replacement drawing sheet for FIG. 1 is attached hereto. FIG. 1 has been amended to include the legend -PRIOR ART-- as suggested by the examiner to satisfy the objection to the drawings.

Claims 12-16 have been amended to correct dependencies as suggested by the examiner to overcome the objection.

Claims 1-6 and 11-16 have been amended to overcome the rejection under 35 U.S.C. § 102(e). Support for the amendment may be found in the specification on page 1, lines 22-25, page 5, lines 6-15, and on page 9, lines 1-3.

Applicant acknowledges with appreciation the notice of allowable subject matter of Claims 7-10 and 17-20; however, Applicant submits that these claims are distinguishable over the prior art of record for reasons not limited to those presented by the examiner, and that the record speaks for itself.

Claims 1-20 are pending in the application.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Timothy R. Croll at (408)433-7625 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 U.S.C. § 102

Claims 1-6 and 11-16 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Dor et al., U.S. Patent 6,701,259 (*Dor*). Applicant traverses the rejection as follows.

Claims 1 and 11 have been amended to recite:

(a) finding a plurality of pre-scan defect locations on a surface of a semiconductor wafer;

(b) subjecting the semiconductor wafer to processing by a process tool after step (a);

(c) finding a plurality of post-scan defect locations on the surface of the semiconductor wafer after step (b); and

(d) calculating which defects were added by the process tool from the pre-scan defect locations and the post-scan defect locations.

The rejection alleges on page 3 that *Dor* teaches the claimed step of finding a plurality of pre-scan defect locations in column 6, lines 25-26 and in FIG. 2, ID (206). However, in column 6, lines 25-26, *Dor* simply teaches using an electron microscope to inspect a semiconductor surface, not finding pre-scan defect locations. Further, *Dor* teaches in column 2, lines 52-63 that the defect source identifier 100 in FIG. 2 including ID (206) identifies defects in a wafer after the wafer has been processed in the wafer processing system 102. Because the defect source identifier 100 in FIG. 2 identifies defects in the wafer after processing in the wafer processing system 102, *Dor* lacks the claimed step of finding a plurality of pre-scan defect locations on a surface of a semiconductor wafer before processing as recited in amended Claims 1 and 11. Because *Dor* lacks the claimed step of finding a plurality of pre-scan defect locations on a surface of a semiconductor wafer, *Dor* does not anticipate Claims 1 and 11 under 35 U.S.C. § 102.

The rejection further argues that *Dor* teaches the claimed step of calculating defects added by the process tool from the pre-scan defect locations and the post-scan defect locations in column 13, lines 51-54 and in FIG. 2, ID 100. However, in column 13, lines 51-54, *Dor* discloses calculating which defects were detected by the tool that most recently inspected the wafer. In contrast to *Dor*, the claimed calculation determines which defects were added by the process tool. In other words, the adders in *Dor* are defects that are detected by an inspection tool, while the adders defined on page 1, lines 22-25 of the specification are recited in Claims

1 and 11 as defects that are added to the wafer by a process tool. Clearly, the adders referred to in *Dor* are not those recited in Claims 1 and 11. Further, *Dor* lacks the claimed step of finding a plurality of pre-scan defect locations on a surface of a semiconductor wafer as explained above. Because *Dor* lacks the claimed step of finding pre-scan defect locations, *Dor* lacks the claimed step of calculating which defects were added by the process tool from the pre-scan defect locations and the post-scan defect locations. Because *Dor* lacks the claimed step of calculating which defects were added by the process tool, *Dor* does not anticipate Claims 1 and 11 under 35 U.S.C. § 102.

Regarding Claims 2 and 12, *Dor* lacks the claimed step of calculating which defects were added by the process tool as explained above. Because *Dor* lacks the claimed step of calculating which defects were added by the process tool, *Dor* lacks the claimed step of displaying a map of the defects added by the process tool.

Regarding Claims 3 and 13, *Dor* lacks the claimed step of calculating which defects were added by the process tool as explained above. Because *Dor* lacks the claimed step of calculating which defects were added by the process tool, *Dor* lacks the claimed step of displaying a scatter plot of a point representative of a total number of defects added by the process tool to the semiconductor wafer.

Regarding Claims 5 and 15, *Dor* lacks the claimed step of calculating which defects were added by the process tool as explained above. Because *Dor* lacks the claimed step of calculating which defects were added by the process tool, *Dor* lacks the claimed added defect map.

Regarding Claims 6 and 16, the rejection fails to show that *Dor* discloses the claimed step of associating a spatial signature of added defects from the added defect map with a process tool malfunction.

Applicant respectfully requests examination and

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favorable reconsideration of Claims 1-20.

No additional fee is believed due for this amendment.

Respectfully submitted,

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encl: Replacement Sheet for FIG. 1

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